Simulated Evaluation of Modern Multilevel Inverter Topologies

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***Abstract* - One of the important components in the electrical system is the inverter which converts the DC energy stored in the battery banks to AC energy that is used by consumers or connected to power grid. As the current trend needed cleaner power supply, higher output power, less losses and almost free from harmonics, people are looking forward for better inverter. A conventional multilevel inverter is no more relevant to cope up with the requirements. Nowadays, to overcome the said problems is the point of concern for industries and researchers. In this paper new multilevel inverter topologies are referred over conventional ones as the quality of output voltages improves with the number of voltage steps at the output. These new topologies utilizes fewer power electronics components to generate a specific number of output voltage levels in comparison with the traditional multilevel inverters resulting in compact, reliable, efficient and economical solution.**

Keywords Multilevel Inverter, Switched Sources, Reduced devices, Total Harmonic Distortion.

I. Introduction

Multilevel inverter technology has been developed recently as alternative in the area of medium and high power applications [9]. Traditional Multilevel Inverters however, exhibit an important limitation for increased number of output levels, they require a large number of power switches, thereby increasing the cost, size and control complexity [4] [5] [6].

Three traditional topologies can be considered for multilevel inverters: diode-clamped, flying capacitors and cascaded H-bridge with separate DC sources structured of electronic switches, capacitors and diodes. Based on the ON/OFF operations of switches, the output voltage can result into step output voltage levels [1], [10]. By increasing the amount of output voltage levels in traditional topologies, the output voltages have additional steps generating a stairs waveform with reduced harmonic distortion [3], [8].

The restrictions of traditional multilevel inverters may cause the overall system to be more expensive, bulky and complex [3]. The above problems should be solved in advance as it is the need of an hour. Here comes the need for a different topology of multilevel inverter which will overcome these problems.

In this paper, different multilevel inverter topologies identified and simulated are (1) Series Connected Switched Sources (SCSS) (2) Switched Series Parallel Sources (SSPS) (3) Multilevel Module Topology (MLM) and (4) Reversing Voltage Topology (RV). These topologies can output numbers of voltage levels with less number of switching devices, which leads to the reduction of the size and cost [2].

The remaining parts of the paper are as follows: Section II describes the identified circuit topologies. Section III describes simulation results with Total Harmonic Distortion (THD) comparison and Section IV concludes the paper.

II. Circuit Topologies

A. Series Connected Switched Sources (SCSS)

Fig. 1 shows the configuration of a nine level Series Connected Switched Sources topology of multilevel inverter.

SCSS topology consists of an H - bridge and an inverter, in which multilevel output is obtained by switching the DC voltage sources in Series. However, the given circuit configuration can generate maximum nine output voltage levels. This topology consists of two parts: Level generation part and Polarity generation part. Switches Q1, Q2, Q3, and Q4 constitute polarity generation part and other S_1 to S_8 switches are for level generation. To generate 9 levels of output voltage this topology uses total 12 switching devices. [2]

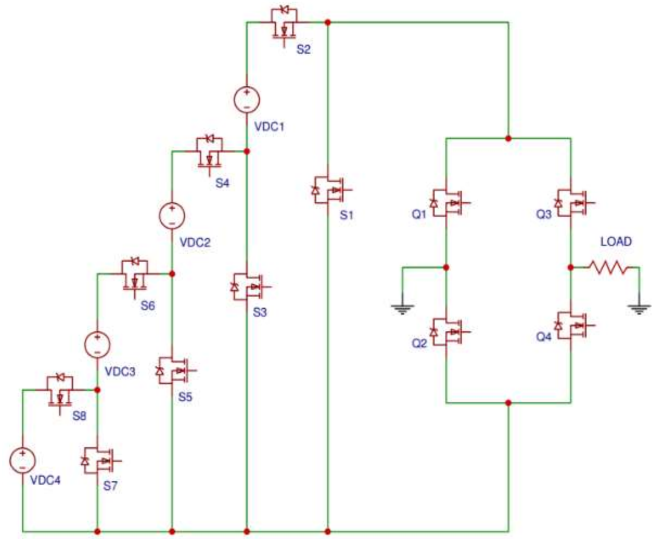

Fig. 1: Series Connected Switched Sources (SCSS) Topology [6], [7]

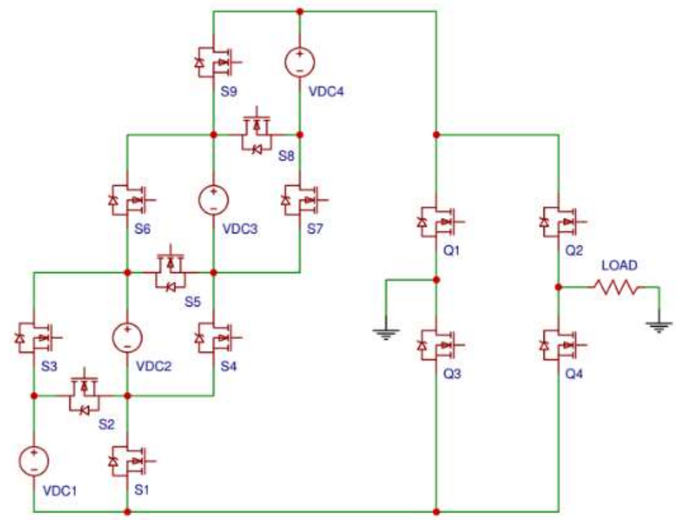

Fig. 2: Switched Series Parallel Sources (SSPS) Topology [4], [5]

TABLE I: SWITCHING COMBINATION FOR SCSS TOPOLOGY (9-LEVEL) [1]

Levels	Voltage Sources	Switches in ON state
1	VDC1	S2, S3
2	VDC1 + VDC2	S2, S4, S5
3	VDC1 + VDC2 + VDC3	S2, S4, S6, S7
4	VDC1 + VDC2+ VDC3+ VDC4	S2, S4, S6, S8
0	GND	S1

To generate 9 output levels, the switching combination is listed in Table I. By proper switching of switches at particular instant required output voltage levels can be generated. Number of redundancies in switching states can be obtained for all levels by different switching combinations except 0 volts, which reduces voltage stress across the devices.

B. Switched Series Parallel Sources (SSPS)

The SSPS topology configuration for 9 levels output voltage is shown in Fig. 2. This topology uses 13 switches to generate 9 levels at output. It also consists of H- Bridge, for polarity generation Q1, Q2, Q3, Q4 switches are used same as that of SCSS. For level generation it uses 9 switches from S_1 to S_9, one extra switch is needed for SSPS compare to SCSS. [4]

TABLE II: SWITCHING COMBINATION FOR SSPS TOPOLOGY (9-LEVEL) [1]

Levels	Voltage Sources	Switches in ON state
1	VDC1	S3, S6, S9
2	VDC1 + VDC2	S2, S6, S9
3	VDC1 + VDC2 + VDC3	S2, S5, S9
4	VDC1 + VDC2+ VDC3+ VDC4	S2, S5, S8
0	GND	Q1, Q2

Switching combinations to obtain 9 output levels are given in Table II. For example, if maximum 2 levels are to be generated at the output, S2, S6, S9 switches are controlled. The H-Bridge Structure in both SCSS and SSPS are made up of four switches Q1, Q2, Q3, and Q4 which plays important role in topologies to decide the polarity. For positive polarity generation Q1, Q4 are controlled at a time and for negative polarity generation Q2, Q3 are controlled.

C. Multilevel Module (MLM)

In Multilevel Module configuration the switches are arranged such that they can block unidirectional and conduct in bidirectional shown in Fig. 3. This can be achieved by connecting the switching devices in anti-series fashion. This topology also consists of two sections; Level generation section and Polarity generation section. Level generation configuration uses anti-series connected switches. S1 to S5 are level generation switches and Q1, Q2, Q3 and Q4 are polarity generation switches. [2]

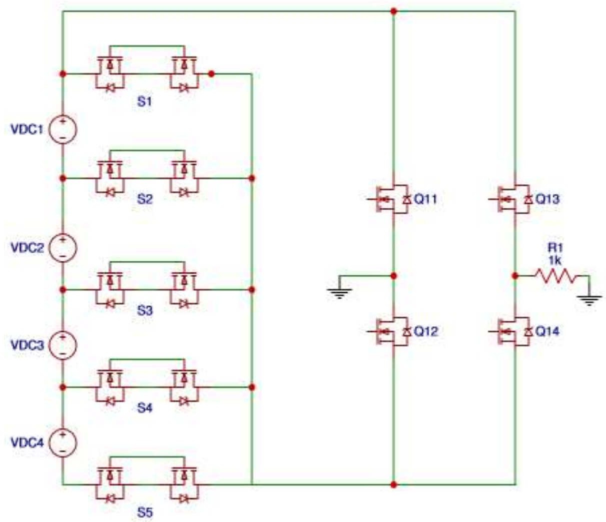

Fig. 3: Multilevel Module Topology for 9-level

TABLE III: SWITCHING COMBINATION FOR MLM TOPOLOGY (9-LEVEL)

Levels	Voltage Sources	Switches in ON state
1	VDC1	S2
2	VDC1 + VDC2	S3
3	VDC1 + VDC2 + VDC3	S4
4	VDC1 + VDC2+ VDC3+ VDC4	S5
0	GND	S1

In MLM configuration, it will not produce correct output for different input voltage levels because it is impossible to generate proper stair case output with it. Switching combination for 9 level output voltage are shown in Table III. For every level generation at output one has to switch only one switching device in ON state. Total count of switches required for this topology is 14.

D. Reverse Voltage (RV)

Reverse Voltage topology has two parts level and polarity like in above mentioned topologies. The reverse word is because to generate voltage levels at output some of the switching devices conduct though the feedback diodes which conduct in opposite direction of the conducting device. Switching Devices S1 to S8 does the work of level generation and Q1, Q2, Q3, and Q4 does the work of polarity generation. The configuration of RV is shown in Fig. 4. [2]

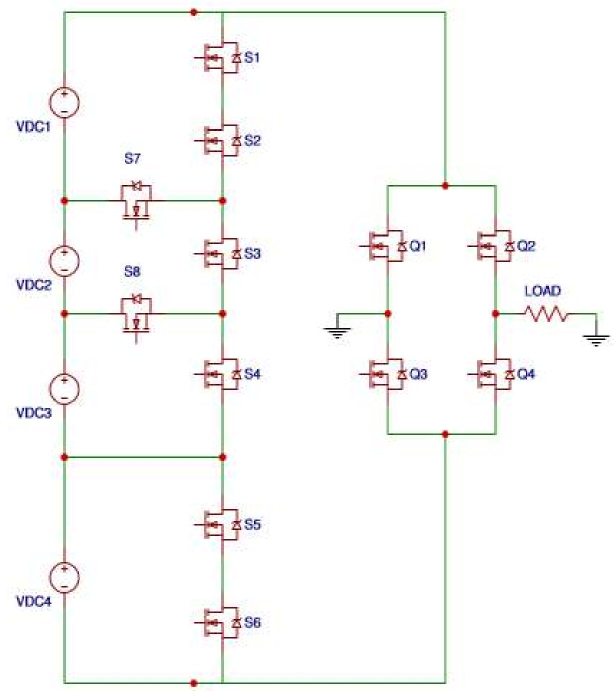

Fig. 4: Reversing Voltage (RV) Topology

Table IV: Switching Combination For RV Topology (9-Level)

Levels	Voltage Sources	Switches in ON state
1	VDC3	S2, S3, S5,S8
2	VDC1 + VDC2	S2, S5, S7
3	VDC1 + VDC2 + VDC3	S2, S6, S7
4	VDC1 + VDC2+ VDC3+ VDC4	S1, S6
0	GND	S2, S3, S4,S5

Table IV shows the switching combination for the RV topology to generate 9 level output voltage. In RV redundancy of voltage levels cannot be obtained for different switching combinations.

III. SIMULATION RESULTS

To determine the practical possibility of the offered multilevel inverter, simulation of circuit is necessary needed.

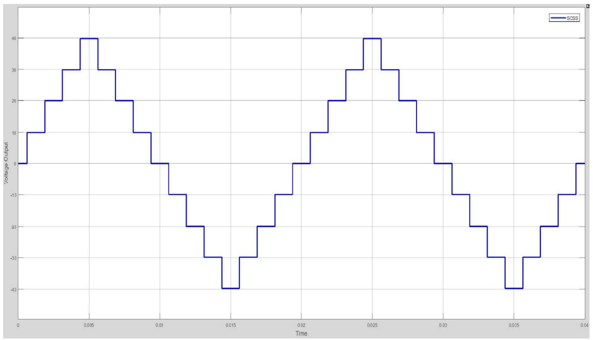

Fig. 5: Simulation Results For SCSS Topology 9-Level

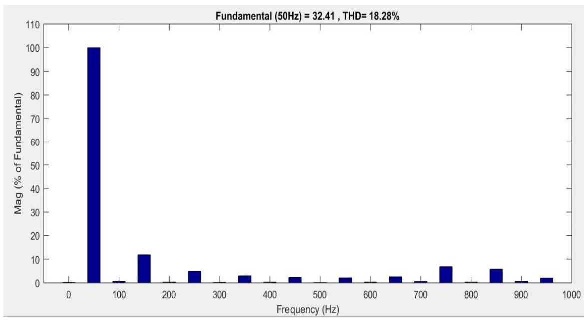

Fig. 6: FFT Analysis of SCSS Results with THD

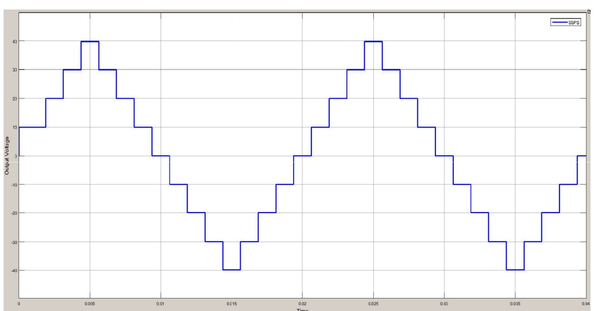

Fig. 7: Simulation Results For SSPS Topology 9-Level

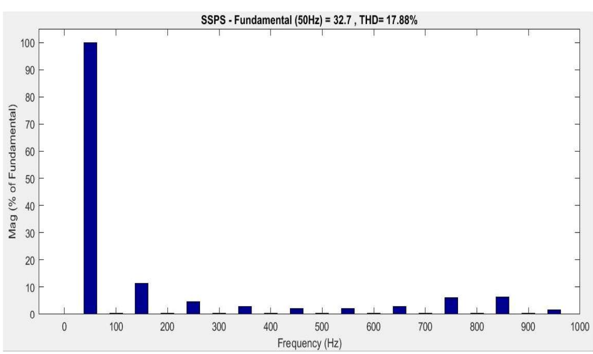

Fig. 8: FFT Analysis of SSPS Result with THD

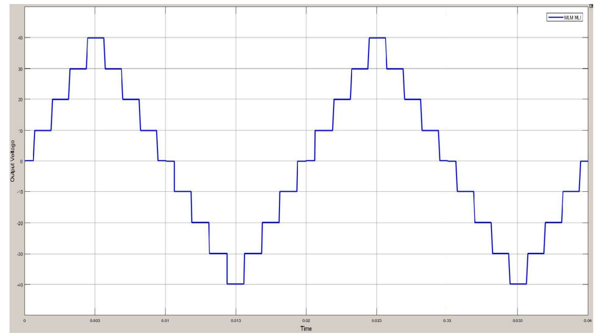

Fig. 9: Simulation Results for MLM Topology 9-Level

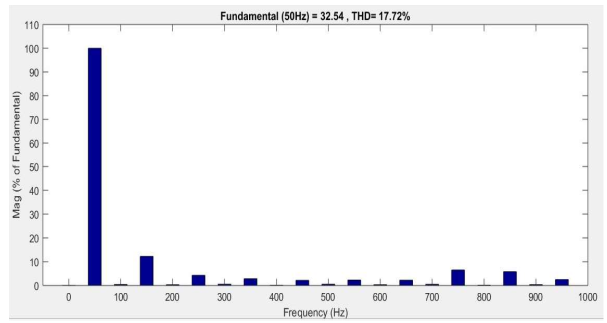

Fig. 10: FFT Analysis of MLM Results with THD

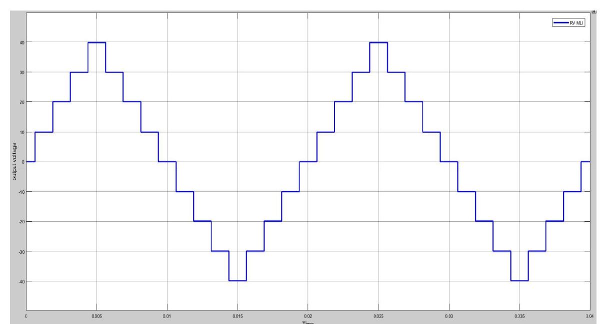

Fig. 11: Simulation Results For RV Topology 9-Level

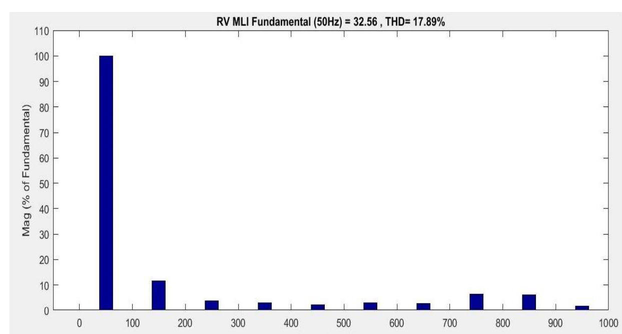

Fig. 12: FFT Analysis of RV Result with THD

Switching combinations in these converters are easier than traditional once. Some additional advantage is that, it does not need any extra circuit for negative pulse generation. There is no need of extra controlling of negative voltage, here the H-bridge will perform this task and the required output voltage is produced by switching devices of higher ratings.

MATLAB/SIMULINK software is used to simulate the circuit and to analyse the operation of the given topologies. For 9-level simulation results switching frequency of 50 Hz is considered. According to it the switching timings are fixed for all the switches. Fig. 5 and Fig. 6 shows the output voltage waveform and THD obtained after Fast Fourier Transform (FFT) analysis of output voltage for SCSS configuration. For SSPS output voltage waveform and THD obtained from FFT analysis of output voltage is shown in Fig. 7 and Fig. 8. Fig. 9 and Fig. 10 shows the output voltage waveform and THD obtained after FFT analysis of output voltage for MLM configuration. For RV output voltage waveform and THD obtained after FFT analysis of output voltage is shown in Fig. 11 and Fig. 12. Configurations are implemented in MATLAB/SIMULINK 2018Ra respectively.

To determine the harmonic content in the obtained result of 9-level inverter topologies, FFT analysis is carried out. Comparison is tabulated in Table V.

TABLE V: COMPARISION RESULT OF TOPOLOGIES

Criteria	SCSS	SSPS	MLM	RV
No. of Levels	9	9	9	9
No. of Switches	12	13	14	12
THD in %	18.28%	19.73%	17.72%	17.89%

IV. CONCLUSION

For 9-level output voltages THD results achieved for topologies are for SCSS configuration the THD is 18.28 %, SSPS configuration the THD is 19.73 %, for MLM configuration THD is 17.72% and for RV configuration the THD is 17.89 %.

When device count reduced with certain complexity in the circuit, THD will increase instead of decreasing. If the configuration is kept simple higher chances of reduction of harmonics are observed along with some other benefits such as compact size, cost effectiveness, reduced power consumption, less requirement of voltage blocking capacity.

Thus, these Converters can discover various applications in industrial system drive, electric vehicle drives and traction drives which are in medium voltage and high power range. One of the major sectors for the multilevel inverter is renewable energy resources where power quality and proficiency are important factor for researchers.

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